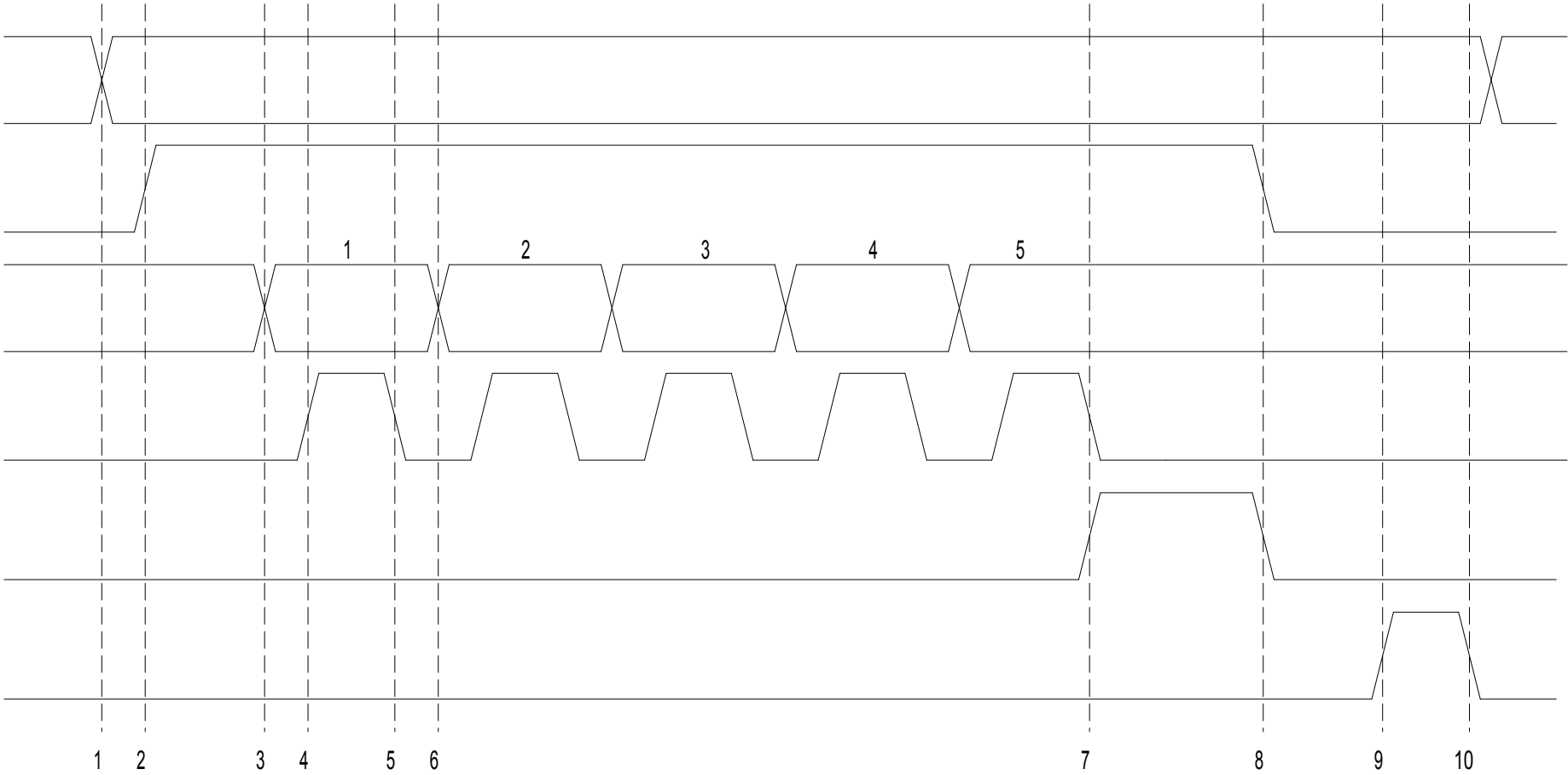


CMS TIMING DIAGRAM

No Scale



NOTE: Logic is Ground True. For this detail, up is True(1) and down is False(0).  
Rise and Fall timer shall stabilize within 10μ seconds.

SEQUENCE OF OPERATION

- |     |  |
|-----|--|
| 1.  | Place Address on Address Lines.  |
| 2.  | Set the Enable Line to True.   |
| 3.  | Begin Data transfer loop, place Data on Data Lines. First word/Fifth row onto Fifth word/First row of Pixels.              |
| 4.  | Set the Clock Line to True. The leading edge will shift data in shift register.  |
| 5.  | Set the Clock Line to False.   |
| 6.  | Place the next Data on the Data Lines and loop until all 5 bytes of data are transferred.                                  |
| 7.  | The trailing edge of the Clock Line will cause the Latch Line to go True.  |
| 8.  | Set the Enable Line to False. The Latch Line will go False.  |
| 9.  | Set the Clear Line to True. This will turn off Pixel Load Triacs and transfer data from shift registers to output latches. |
| 10. | Set the Clear Line to False. This enables Pixel Load Triacs with new message.  |